ABSTRACT OF THE DISCLOSURE

An integrated circuit adapted for ECO and FIB debug comprises: a substrate, a spare cell, a top-layer output terminal pad and a top-layer output terminal pad. The spare cell is disposed in substrate and comprises at least one input terminal and at least one output terminal. The top-layer output terminal pad and the top-layer input terminal pad are disposed in a top metal layer. The top metal layer is disposed over the substrate. The top-layer output terminal pad and the top-layer input terminal pad are electrically coupled to the output terminal and input terminal of the spare cell by a via structure, respectively.